WHAT IS CLAIMED IS:

1. A tester for a semiconductor device, comprising:

a bottom ground pad structure electrically connected to a substrate, the bottom ground pad structure comprising a bottom signal shield plate;

an intermediate ground pad structure electrically connected to the bottom ground pad structure, the intermediate ground pad structure being located over the bottom ground pad structure; and

a top layer located over the intermediate ground pad structure, the top layer comprising a device under test (DUT), a ground probe pad, a signal probe pad, and leads, wherein the DUT is electrically connected to the ground probe pad and the signal probe pad via the leads, wherein the ground probe pad is electrically connected to the intermediate ground pad structure, and wherein the signal probe pad is located over the bottom signal shield plate.

2. The tester of claim 1, further comprising a bottom series of contacts located between the bottom ground pad structure and the substrate, wherein the bottom ground pad structure is electrically connected to the substrate via the bottom series of contacts.

3. The tester of claim 1, further comprising an intermediate series of contacts located between the bottom ground pad structure and the intermediate ground pad structure, wherein the intermediate ground pad structure is electrically connected to the bottom ground pad structure via the intermediate series of contacts.

4. The tester of claim 1, further comprising a top series of contacts located between the intermediate ground pad structure and the top layer, wherein the ground probe pad is electrically connected to the intermediate ground pad structure via the top series of contacts.

5. The tester of claim 1, further comprising:

another ground probe pad located in the top layer; and

an inter-ground connecting line extending between the ground probe pads, wherein the ground probe pads are electrically connected to each other via the inter-ground connecting line.

6. The tester of claim 5, wherein the inter-ground connecting line has about a same width as the ground probe pads.

7. The tester of claim 5, wherein at least one of the leads is electrically connected between the inter-ground connecting line and the DUT, wherein the ground probe pads are electrically connected to the DUT via the inter-ground connecting line.

8. The tester of claim 1, wherein the intermediate ground pad structure comprises two corner portions and an inter-ground connecting line, wherein the inter-ground connecting line extends between and electrically connects the two corner portions.

9. The tester of claim 8, wherein the inter-ground connecting line has a smaller width than the corner portions.

10. The tester of claim 8, wherein each of the corner portions has a plate shape.

11. The tester of claim 8, wherein each of the corner portions has a hollow box shape.

12. The tester of claim 1, further comprising a second intermediate ground pad structure located between the bottom ground pad structure and the top layer, wherein the second intermediate ground pad structure is electrically connected to the ground probe pads and the bottom ground pad structure.

13. A tester for a semiconductor device, comprising:

a bottom layer comprising a bottom ground pad structure, the bottom ground pad structure being electrically connected to a substrate via a bottom series of contacts, the bottom ground pad structure comprising a bottom signal shield plate;

at least one intermediate layer, each intermediate layer comprising an intermediate ground pad structure, the intermediate ground pad structure being electrically connected to the bottom ground pad structure via an intermediate series of contacts; and

a top layer comprising a device under test (DUT), a ground probe pad, a signal probe pad, and leads, wherein the DUT is electrically connected to the ground probe pad and the signal probe pad via the leads, wherein the ground probe pad is electrically connected to an uppermost one of the at least one intermediate ground pad structure via a top series of contacts, and wherein the signal probe pad is located over the bottom signal shield plate.

14. The tester of claim 13, further comprising:

another ground probe pad located in the top layer; and

an inter-ground connecting line extending between the ground probe pads, wherein the ground probe pads are electrically connected to each other via the inter-ground connecting line.

15. The tester of claim 14, wherein the inter-ground connecting line has about a same width as the ground probe pads.

16. The tester of claim 14, wherein at least one of the leads is electrically connected between the inter-ground connecting line and the DUT, wherein the ground probe pads are electrically connected to the DUT via the inter-ground connecting line.

17. The tester of claim 13, wherein the intermediate ground pad structure comprises two corner portions and an inter-ground connecting line, wherein the inter-ground connecting line extends between and electrically connects the two corner portions.

18. The tester of claim 17, wherein the inter-ground connecting line has a smaller width than the corner portions.

19. The tester of claim 17, wherein the corner portion has a plate shape.

20. The tester of claim 17, wherein the corner portion has a hollow box shape.

21. A tester for a semiconductor device, comprising:

a bottom layer comprising a bottom ground pad structure, the bottom ground pad structure being electrically connected to a substrate via a bottom series of contacts, the bottom ground pad structure comprising:

four bottom corner portions, and

two bottom signal shield plates, wherein each bottom signal shield plate extends between and electrically connects two of the bottom corner portions;

at least one intermediate layer, each intermediate layer comprising an intermediate ground pad structure, the intermediate ground pad structure being electrically connected to the bottom ground pad structure via an intermediate series of contacts, the intermediate ground pad structure comprising:

four intermediate corner portions, each intermediate corner portion being located over one of the bottom corner portions, and

two intermediate inter-ground connecting lines, wherein each intermediate inter-ground connecting line extends between and electrically connects two of the intermediate corner portions, and wherein each intermediate inter-ground connecting line has a smaller width than the intermediate corner portions; and

a top layer comprising a device under test (DUT), four ground probe pads, two top inter-ground connecting lines, two signal probe pads, and leads, wherein the DUT is electrically connected to the ground probe pads and the signal probe pads via the leads, wherein the ground probe pads are electrically connected to an uppermost one of the at least one intermediate ground pad structure via a top series of contacts, wherein each signal probe pad is located over one of

the bottom signal shield plates, and wherein each ground probe pad is located over one of the intermediate corner portions.

22. The tester of claim 21, wherein each intermediate corner portion has a plate shape.

23. The tester of claim 21, wherein each intermediate corner portion has a hollow box shape.